

CLAIMS

What is claimed is:

12. In a wireless receiver, a method for DFT processing a selected number P of midamble data values, where P has a plurality of relatively prime factors N_i , for $i = 1$ to M , where $\prod_{i=1}^M N_i = P$, comprising the steps:

storing P data values in a memory;

inputting P data values at a control circuit from said memory for M consecutive iterations, one for each factor N_i , such that $K=N_i$ and P/N_i groups of data values are processed for each iteration; and

DFT processing, by selectively controlled DFT processing circuitry, data values in groups of a selected number K , comprising:

storing twiddle sets in first and second twiddle registers associated with DFT processing of all factors N_i ;

receiving in a first cache L selected values of each group of K data values, where $L \geq K/2$;

receiving in a second cache $K-L$ other data values of each group of K values such that the processing of the data values received in the second cache has twiddle sets symmetrical to some of the data values received in the first cache;

processing, by a first prime factor algorithm (PFA) circuit, K data value groups received from said first and second caches and said first twiddle register; and

processing, by a second PFA circuit, the same K data value groups in tandem with said first PFA circuit using a twiddle sets from said second twiddle register.

13. The invention of claim 12 wherein said processing further comprises combining outputs of the first and second PFA circuits for output by said processing circuitry.

14. The invention of claim 12 further comprising outputting the DFT processed data to said memory, whereby each successive N point DFT processing of the stored P data values processes the values output from a prior DFT processing iteration.

15. The invention of claim 14 wherein $P=456$, $M=3$, $N_1=3$, $N_2=8$, $N_3=19$.

16. The invention of claim 15 wherein $K=N_1$ for a first DFT processing iteration, $K=N_2$ for a second DFT processing iteration and $K=N_3$ for a third DFT processing iteration.

17. The invention of claim 14 wherein $P=192$, $M=2$, $N_1=3$ and $N_2=64$.